


Memristor fabrication

JT Jianshi Tang

Updated date: Nov 12, 2020

 An abbreviated version of this protocol was published in Science Advances in Oct 2020

Multichannel parallel processing of neural signals in memristor arrays

DOI: 10.1126/sciadv.abc4797

Detailed protocol

For the fabrication of memristor array with one-transistor-one-resistor (1T1R) unit cell, the transistors and peripheral circuits were first fabricated in a commercial foundry with 130nm CMOS process. The foundry process stopped at the patterning of TiN, which served as bottom electrodes for memristors. After that, the following process was used to finish the memristor fabrication:

1. Removing surface oxide on TiN by dilute hydrofluoric acid.
2. Depositing 8nm HfO_x layer by atomic layer deposition.
3. Depositing 40-60 nm TaO_y layer by reactive sputtering.
4. Depositing 20nm TiN layer as top electrodes by sputtering.
5. Depositing 200-500nm Al layer as interconnected wires and pads by sputtering.
6. Patterning interconnected wires and pads by photolithography.
7. Dry etching the Al/TiN/TaO_y/HfO_x stack with Cl₂/BCl₃ plasma.
8. Removing photoresist.

How to cite: (Readers should cite both the Bio-protocol preprint and the original research article where this protocol was used)

1. Tang, J. (2020). Memristor fabrication. Bio-protocol Preprint. bio-protocol.org/prep623.
2. Liu, Z., Tang, J., Gao, B., Li, X., Yao, P., Lin, Y., Liu, D., Hong, B., Qian, H. and Wu, H.(2020). Multichannel parallel processing of neural signals in memristor arrays . Science Advances 6(41). DOI: [10.1126/sciadv.abc4797](https://doi.org/10.1126/sciadv.abc4797)

Copyright: Content may be subjected to copyright.